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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,708	08/08/2002	Gary D. Carpenter	BUR920020011	1884

30449 7590 10/03/2003

SCHMEISER, OLSEN + WATTS
SUITE 201
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LATHAM, NY 12033

EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,708	CARPENTER ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears n the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-17* is/are allowed.

6)☒ Claim(s) *1-7,18 and 19* is/are rejected.

7)☒ Claim(s) *8 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Nojiri (US PAT No. 6,445,210).

Regarding claims 1 and 18, Fig. 8 of Nojiri teaches an I/O driver or a method of maintaining the output states of an I/O driver comprising a circuit adapted to be powered by a first power supply (VDD3), the circuit adapted to receive a first signal referenced to the voltage of a second power supply (VDD) and adapted to convert the first signal to a second signal (output at FF) of the same logic values as the first signal and referenced to the voltage of the first power supply, the circuit adapted to maintain

the second signal on an output of the I/O driver when the second power supply is powered off (FF inherently maintains the output with VDD removed).

Regarding claims 2 and 19, Fig. 8 of Nojiri teaches the I/O driver of claim 1 and the method of claim 18 where the voltage of the first power supply is higher than the voltage of the second power supply (col. 6, lines 56-67).

Regarding claim 3, Fig. 8 of Nojiri teaches the I/O driver of claim 2 where the voltage of the first power supply is 2.5 V or higher (VDD3=3.3V).

Regarding claim 4, Fig. 8 of Nojiri teaches the I/O driver of claim 1 where the circuit includes a level shifting circuit (Fig. 8).

Regarding claim 5, Fig. 8 of Nojiri teaches the I/O driver of claim 4 where the level shifting circuit further includes a latching circuit (FF latches the input signal).

Regarding claim 6, Fig. 8 of Nojiri teaches the I/O driver of claim 1 where the circuit includes a latching circuit (FF latches the input signal).

Regarding claim 7, Fig. 8 of Nojiri teaches the I/O driver of claim 1 includes an output circuit (FF latches and output the input signal) coupled to an I/O pad of an integrated circuit chip (output of FF inherently to input pad of an another circuit).

Allowable Subject Matter

3. Claims 9-17 are allowable over the prior art of record.

4. Claims 8 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although, Nojiri discloses a level shifter circuit, Nojiri differs from the present claimed invention because, among other things, Nojiri pertains to a level shifter with a latch whereas the present claimed invention pertains to specifics of a fencing circuit receiving a fencing signal and controlling latching of the second signal and specifics of first and second latch circuits coupled to the first and second circuit where the first and second latches maintain the logical state of its output when the second power supply is powered off and the output of the latches are coupled to a combinational logic circuit and the output of the logic circuit is maintained when the second power supply is powered off. Accordingly, one of ordinary skill in the art would not have been motivated to modify the teachings of Nojiri to meet the claimed limitation as set forth in the present claimed invention.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yano (US PAT No. 6,323,687) discloses output drivers with VCCQ supply compensation.

Noda (US PAT No. 6,094,083) discloses voltage converting buffer circuit capable of realizing high speed flip-flop action in the flip-flop circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

James H. Cho
Examiner
Art Unit 2819

September 22, 2003